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Title: Evaluation of Power Costs in Triplicated FPGA Designs

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Evaluation of Power Costs in Triplicated FPGA Designs

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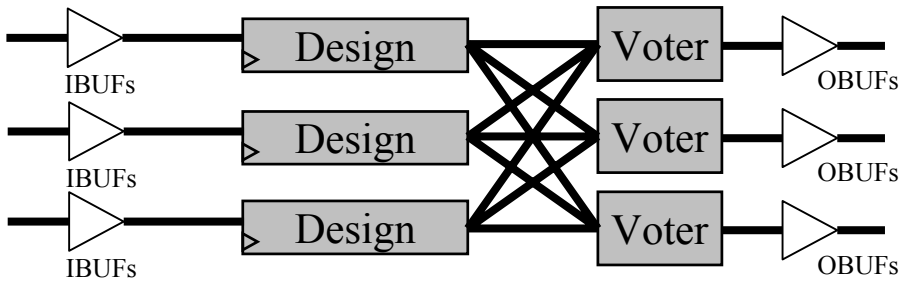
Area and Speed Costs of TMR

- Bulletproof design is possible with 3-voter TMR



- Area Cost: 3x – 6x
- Speed Cost: up to 50% slower

Power Costs of TMR

- FPGAs consume relatively more power than ASICs
- TMR may cause a triplication of an already large power consumption

- Goal: Investigate the cost of TMR in terms of power consumption

JPower

- Tool to measure total current on SLAAC1V board (in mA)
- Current Measurments:
  - 2.5V channel sampled at 120 kHz
  - Current stored in a register as a 10-bit number
    - Value in register multiplied by 4.8828125 mA and rounded to the nearest mA
    - Max current reading: 4990mA
- Averaged current measurements are repeatable to within a few mA

XPower

- Xilinx power measurement tool
- Requires:
  - *.ncd and *.pcf files or *.par.ncd file
  - Activity rates for EVERY net in the design
    - 3 ways to assign net activity rates:
      - Manually in the XPower tool (GOOD LUCK!)
      - Import *.xml file
      - Import *.vcd or *.xad files

Calibrating JPower and XPower

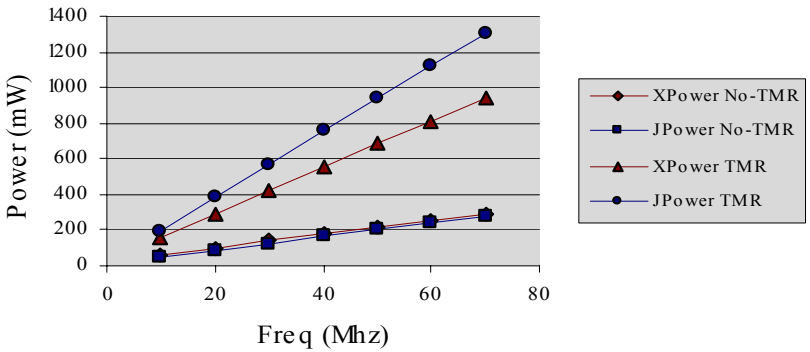
- Blank Design – run JPower with no designs on SLAAC1V board (default X0 design)
  - Run JPower tool with and without clock running at frequencies from 10MHz – 100MHz
  - Results from this blank design provides an equation which allows us to isolate the power measurements to a single FPGA on the SLAAC1V board

Test Calibration

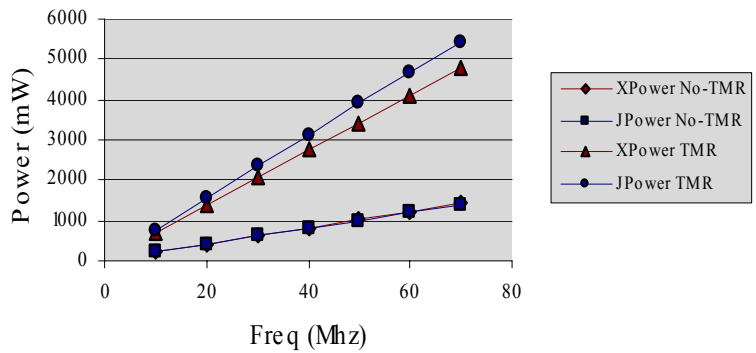
- Four 8-bit Designs (non-TMR & TMR):
  - **Incrementer**
    - 72 incrementers – each output to IOBs
  - **XOR'ed Incrementer**
    - 416 incrementers – groups of outputs XOR'ed
  - **Up/Down Loadable Counter**
    - 416 counters – final counter bits output to IOBs
  - **3 CLK** Implementations of above designs

Calibration Results

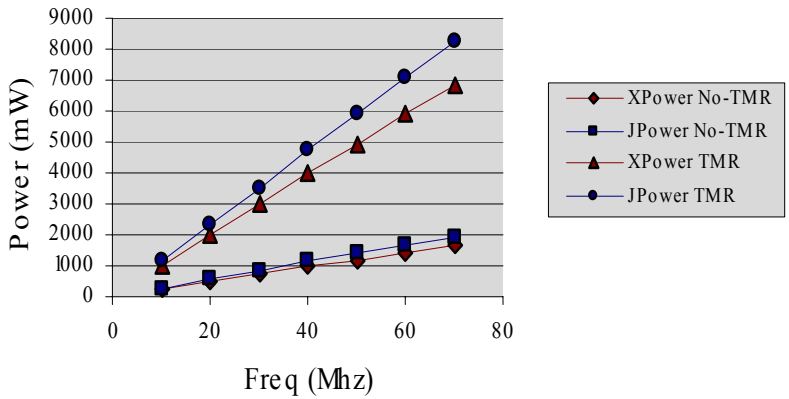
Incrementer Auto-Placed



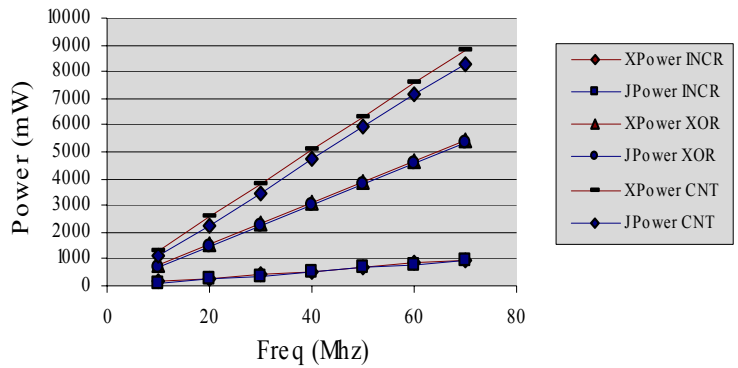
XOR Incrementer Auto-Placed



Counter Auto-Placed



3-CLK Auto-Placed



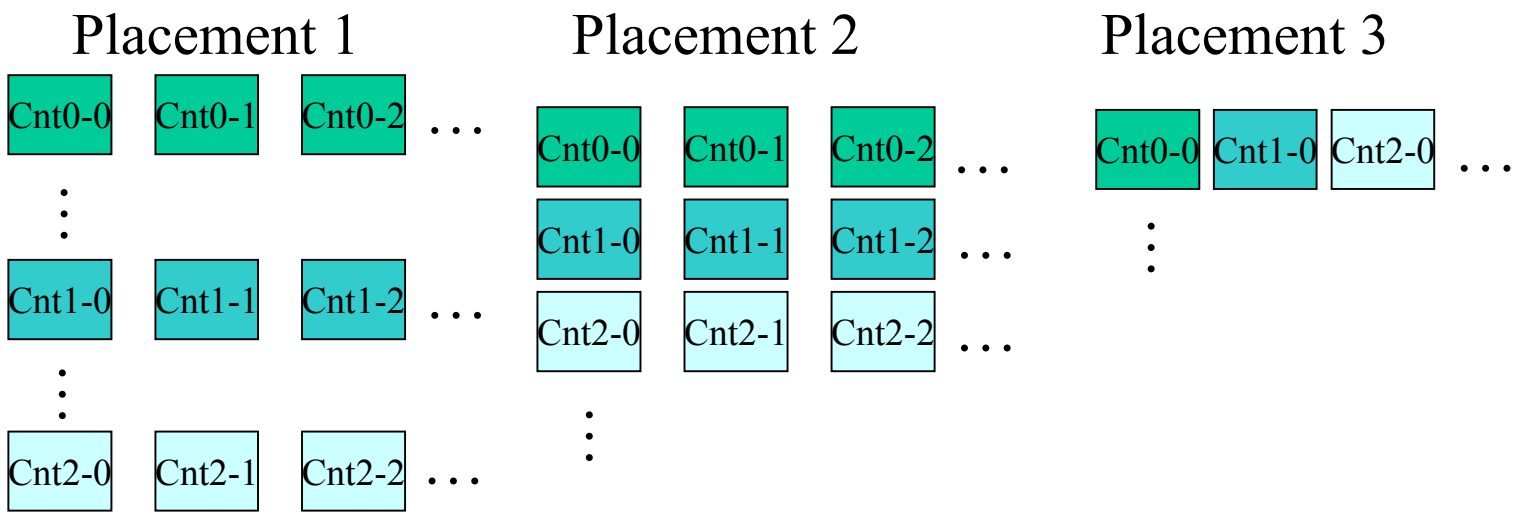
Calibration Results

- "Close" match between JPower & XPower for non-TMR designs and for TMR designs with triplicated clock
- Large slope difference in counter TMR design

	Non - TMR			TMR			3 CLK (TMR)		
	INC	**XOR**	**CNT**	**INC**	**XOR**	**CNT**	**INC**	**XOR**	**CNT**
Frequency vs. Power Slopes									
JPower	1.54	7.85	11.08	7.37	31.13	47.53	5.37	30.67	48.14
XPower	1.54	7.95	9.26	5.23	27.06	39.03	5.28	30.62	49.94
Area Costs									
LUTs	576	3250	3328	1728	9750	19968	1728	9750	19968

Effects of Design Placement on Power Consumption

- Incrementer TMR design used to test effects of placement on power
  - 3 different placements used:



Effects of Placement

- Comparison of frequency vs. power slopes for auto-placed and hand-placed designs shows the effects of placement
- "JP/XP" row ratio indicates how closely JPower and XPower match

	Incrementer		XOR Incrementer		Up/Down Counter	
	Auto-Place	**Hand-Place**	**Auto-Place**	**Hand-Place**	**Auto-Place**	**Hand-Place**
Frequency vs. Power Slopes						
JPower	7.37	4.78	31.13	22.18	47.53	41.22
XPower	5.23	4.76	27.06	25.10	39.03	36.40
JP / XP	1.41	1.00	1.15	0.88	1.22	1.13

Effects of Placement

- JPower is much more sensitive to placement than Xpower
- JPower and XPower closest with placement 3 (optimized hand-placement)

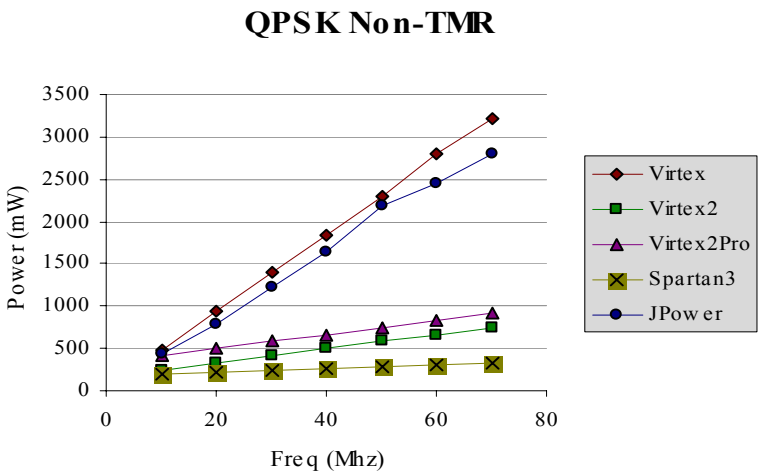
	Auto-Place	Place 1	Place 2	Place 3
Frequency vs. power slopes (TMR)				
JPower	7.37	10.65	6.15	4.76
XPower	5.23	6.20	5.21	4.78
Power increase due to TMR (TMR / non-TMR)				
JPower	4.79x	7.04x	4.06x	3.15x
XPower	3.40x	4.04x	3.39x	3.10x

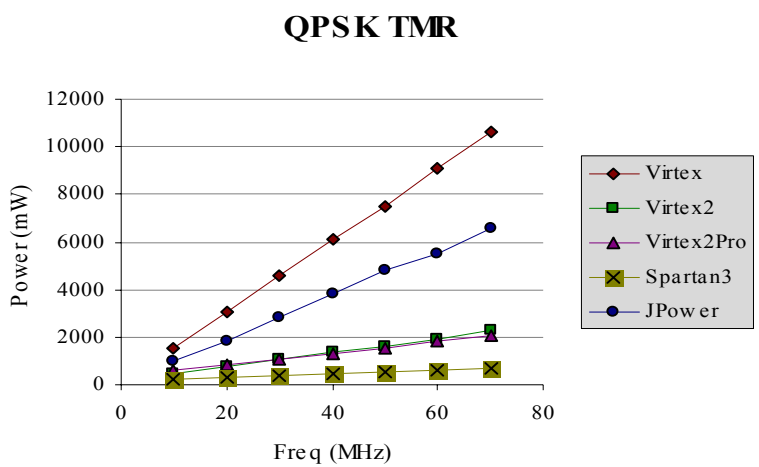
Realistic Designs: Area and Speed Costs

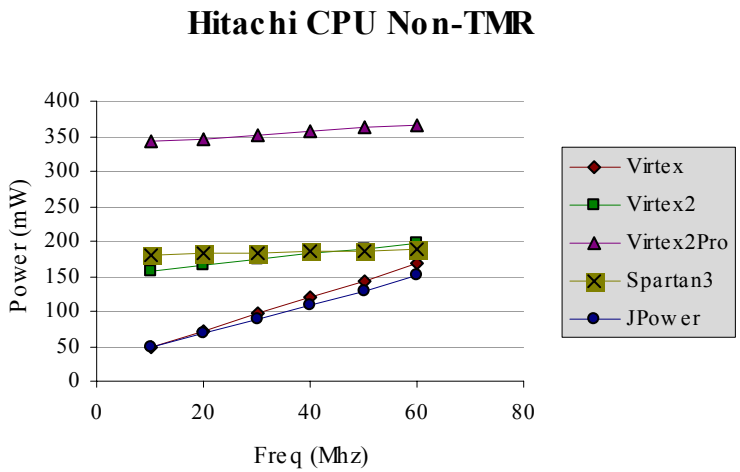
		QPSK Demodulator	Hitachi CPU
Virtex	**TMR Area Cost**	3.03x	3.01x
	TMR Speed Cost	95.2 %	71.1 %
Virtex2	**TMR Area Cost**	3.03x	3.00x
	TMR Speed Cost	84.6 %	100.0 %
Virtex2Pro	**TMR Area Cost**	3.03x	3.00x
	TMR Speed Cost	77.9 %	80.8 %
Spartan 3	**TMR Area Cost**	3.02x	3.00x
	TMR Speed Cost	97.2%	87.0 %

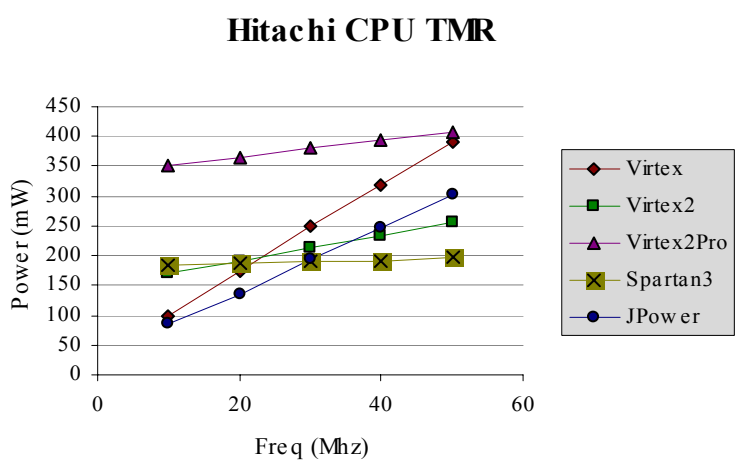
Area and speed costs due to TMR

Realistic Designs: Power Costs









Realistic Designs: Power Costs

		Non - TMR					TMR				
		JPower	Virtex	Virtex2	Virtex2Pro	Spartan3	JPower	Virtex	Virtex2	Virtex2Pro	Spartan3
Dynamic Power (mW)	QPSK	40.50	45.71	8.60	8.16	1.97	93.75	150.64	30.17	24.98	6.68
	Hitachi	2.06	2.34	0.79	0.48	0.12	5.48	7.30	2.10	1.39	0.30
Static Power (mW)	QPSK	28.57	22.14	150	336.86	179.83	26.43	37.86	139.5	334.71	182.23
	Hitachi	27.17	26.43	150	337.07	180.00	28.25	27.50	150	337.50	180.34

NOTE: JPower measures power on Virtex parts only

	JPower	Virtex	Virtex2	Virtex2Pro	Spartan3
Dynamic Power Increase Due to TMR (TMR / non-TMR)					
QPSK	2.53x	3.30x	3.51x	3.06x	3.39x
Hitachi	2.66x	3.12x	2.66x	2.88x	2.50x

Power Study Results

- Power consumption increase due to TMR: ~3x
  - Poor design mapping can cause higher power consumption
- Static power can be a significant contribution to total power consumption
- FPGA architecture is significant in determining power consumption